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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,475	02/01/2002	Edward Colles Nevill	1103179-0009	5943

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PATENT DEPARTMENT
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EXAMINER	
COULTER, KENNETH R	

ART UNIT	PAPER NUMBER
2141	3

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,475	NEVILL, EDWARD COLLES	
	Examiner	Art Unit	
	Kenneth R Coulter	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Reissue Applications

1. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,021,265 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

2. Claims 1 – 64 are rejected under 35 USC 251 as lacking basis for reissue, because by statute a reissue application can only be granted for the unexpired portion of the term of the original patent. In re Morgan, 990 F.2d 1230, 26 USPQ2d 1392 (Fed. Cir. 1983).

The patent term has expired due to nonpayment of maintenance fees in the original Pat. No. 6,021,265. To reinstate the original patent, a petition for retroactive payment of maintenance fees must be filed in the original U.S. Pat. No. 6,021,265.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (U.S. Pat. No. 5,542,059) (Dual Instruction Set Processor Having a Pipeline with a Pipestage Functional Unit that is Relocatable in Time and Sequence Order) in view of Blomgren et al. (U.S. Pat. No. 5,781,750) (Dual-Instruction Set Architecture CPU with Hidden Software Emulation Mode).

4.1 Regarding claim 1, Blomgren discloses a data processing apparatus comprising:

(a) a processor core operable to execute successive program instruction words of a predetermined plurality of instruction sets stored in a data memory (Fig. 4; col. 6, lines 29 – 44; col. 6, lines 49 - 64);

(b) a program counter register for indicating an address of a next program instruction word in said data memory (Fig. 4; col. 8, lines 41 – 43; also see in '750 patent, Instruction Pointer IP 12 in Fig. 1 and IPTR 34 in Fig. 2);

(c) logic operable to modify the contents of said program counter register in response to a current program instruction word (Fig. 4; also see in '750 patent, Figs. 1

and 2. Additionally, it was well known in the art that a program counter in a microprocessor has a program counter register modifier.);

(d) a processor core controller, responsive to one or more predetermined indicator bits of said program counter register, operable to control said processor core to execute program instruction words of a current instruction set selected from said predetermined plurality of instruction sets and specified by the state of said one or more indicator bits of said program counter register (Fig. 4; col. 8, line 41 – col. 10, line 29; As acknowledged by Nevill (U.S. Pat. No. 6,021,265) at col. 5, lines 7 – 13 and 56 – 64; it was well known that a program counter does not use the least significant bit in the counter when the processor's smallest instruction is 16 bits and , thus, it would have been obvious that the least significant bit could be used for a specific purpose, such as a mode bit select between two instruction modes for processing like mode 60 in Blomgren (U.S. Pat. No. 5,542,059));

(e) a memory access controller operable to access program instruction words stored in said data memory, said access controller not being responsive to said one or more indicator bits of said program counter register (As acknowledged by the '265 patent at col. 5, line 37 – col. 6, line 4, preventing the supply of a specific bit or bits of an address to a memory in a memory address decoding process was well known in the art.).

4.2 Per claim 2, Blomgren teaches the following additional features:

a first instruction decoder for decoding program instruction words of a first instruction set (Fig. 4, item 32 "CISC ID"; col. 8, lines 41 - 53); and

a second instruction decoder for decoding program instruction words of a second instruction set (Fig. 4, item 32 "CISC ID"; col. 8, lines 41 - 53);

and in which said processor core controller is operable to control either said first instruction decoder or said second instruction decoder to decode a current program instruction word (Fig. 4; col. 8, lines 66 – col. 10, line 29).

4.3 Regarding claim 3, Blomgren discloses program instruction words of said first instruction set are X-bit program instruction words (col. 6, lines 57 – 64; col. 8, lines 47 - 53); and

program instruction words of said second instruction set are Y-bit program instruction words (col. 6, lines 57 – 64; col. 8, lines 47 - 53);

Y being different to X (col. 6, lines 57 – 64; col. 8, lines 47 - 53).

4.4 Per claim 4, the rejection of claim 3 under 35 USC 103 (paragraph 4.3 above) applies fully.

4.5 Regarding claims 5 and 6, Blomgren discloses that Y is 16 and X is 32 (col. 8, lines 51 - 53).

4.6 Per claim 7 , Blomgren teaches that said one or more indicator bits of said program counter register are one or more most significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

4.7 Per claim 8, Blomgren teaches that said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

4.7 Regarding claims 9 - 13, Blomgren discloses that said one or more indicator bits of said program counter register are one or more least significant bits of said program counter register (see details of the rejection of claim 1, item (d) above).

4.8 Per claim 14, Blomgren teaches a data memory for storing program instruction words to be executed (Fig. 4; col. 8, lines 41 - 43).

4.9 Regarding claims 15 – 64, the rejection of claims 1 – 14 under 35 USC 103 (paragraphs 4.1 – 4.8 above) applies.
In addition, Blomgren discloses setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits (Figs. 4, 5, item 42 "control logic"; col. 9, line 60 – col. 10, line 14).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth R Coulter whose telephone number is 703 305-8447. The examiner can normally be reached on 5 4 9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on 703 305-4003. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KENNETH R. COULTER
PRIMARY EXAMINER

krc